CLAIMS

Having thus described the aforementioned invention, we claim:

1. An inductance measurement circuit for measuring an inductance of a wire-loop, said inductance measure circuit comprising:

a pair of resistance-inductance-capacitance driver circuits in electrical communication with a wire-loop;

a demodulation circuit in electrical communication with said pair of resistance-inductance capacitance driver circuits;

a filter in electrical communication with said demodulation circuit, said filter producing a filtered signal; and

an analog-to-digital converter in electrical communication with said filter, said analog-to-digital converter producing a digitized signal representing an inductance measured on the wire-loop.

2. The inductance measurement circuit of Claim 1 further comprising an amplifier circuit in electrical communication between said filter and said analog-to-digital converter, said amplifier producing an amplified signal.

3. The inductance measurement circuit of Claim 1 further comprising a pre-amplifier circuit in electrical communication between said pair of resistance-inductance-capacitance driver circuits and said demodulation circuit.

4. The inductance measurement circuit of Claim 1 wherein said pair of resistance-inductance-capacitance driver circuits operate at a fixed-frequency.

5. The inductance measurement circuit of Claim 1 wherein said demodulation circuit includes a demodulation oscillator, said demodulation circuit producing an output derived from said pair of resistance-inductance-capacitance driver circuits and said demodulation oscillator.

6. The inductance measurement circuit of Claim 5 wherein said output is a demodulated signal corresponding to an envelope of the combined RLC waveform.

7. The inductance measurement circuit of Claim 1 wherein said filter is a bandpass filter which removes noise substantially outside a baseband frequency of the inductance measurement circuit.

8. The inductance measurement circuit of Claim 1 wherein said demodulation circuit is a synchronous demodulator.

9. The inductance measurement circuit of Claim 8 wherein said synchronous demodulator includes a plurality of analog switches.

10. The inductance measurement circuit of Claim 8 wherein said demodulation circuit and said pair of resistance-inductance-capacitance driver circuits operate at substantially similar frequencies.

11. The inductance measurement circuit of Claim 1 further comprising a dc voltage offset generator for producing a dc offset voltage and a signal conditioning circuit in electrical communication between said filter and said dc voltage offset generator, said signal conditioning circuit removing said dc voltage from said filtered signal thereby allowing said filtered signal to be amplified without saturating.

12. The inductance measurement circuit of Claim 1 wherein said pair of resistance-inductance-capacitance driver circuits include a pair of resistance-capacitance networks, each of said pair of resistance-capacitance networks driven by a multi-state buffer, each of said pair of resistance-capacitance networks having a resistance.

13. The inductance measurement circuit of Claim 12 wherein each of said pair of resistance-capacitance networks has a large apparent impedance.

14. The inductance measurement circuit of Claim 12 wherein each of said pair of resistance-capacitance networks is balanced using said multi-state buffer to modulate said resistance.

15. The inductance measurement circuit of Claim 14 wherein said multi-state buffer is driven at a high rate compared to a desired sinusoidal frequency by a duty cycle controlled voltage.

16. The inductance measurement circuit of Claim 1 wherein the wire-loop is directly coupled to said pair of resistance-inductance-capacitance driver circuits.

17. The inductance measurement circuit of Claim 1 further comprising a transformer coupling the wire-loop to said pair of resistance-inductance-capacitance driver circuits, said transformer rejecting a common-mode noise originating from the wire-loop.

18. The inductance measurement circuit of Claim 1 wherein said analog-to-digital converter is a delta-sigma analog-to-digital converter.

19. The inductance measurement circuit of Claim 1 wherein said pair of resistance-inductance-capacitance driver circuits is driven by a differential, periodic waveform.

20. The inductance measurement circuit of Claim 19 wherein said periodic waveform is a sine wave.

21. The inductance measurement circuit of Claim 19 wherein said periodic waveform is a square wave, said square wave having a frequency substantially similar to an operating frequency of said pair of resistance-inductance-capacitance driver circuits.

22. The inductance measurement circuit of Claim 1 wherein said dc offset generator includes a digital-to-analog converter.

23. The inductance measurement circuit of Claim 1 wherein said dc offset generator uses pulse width modulation to adjust a duty cycle of a square wave.

24. The inductance measurement circuit of Claim 1 wherein said analog-to-digital converter includes a voltage reference input, said inductance measurement circuit further comprising a signal generator connected to said voltage reference input, an output of said signal generator selected to match a characteristic of internal noise in said inductance measurement circuit.

25. The inductance measurement circuit of Claim 1 wherein a plurality of said inductance measurement circuits are operating in close proximity, each of said plurality of said inductance measurement circuits operating at a unique carrier frequency and in a distinct frequency band from other closely proximate said inductance measurement circuits.

26. The inductance measurement circuit of Claim 25 wherein each said carrier frequency is separated from each said carrier frequency of a proximate said inductive measurement circuit to provide sufficient bandwidth for operation.

27. The inductance measurement circuit of Claim 25 wherein each said carrier frequency is separated from each other said carrier frequency by between approximately 50 to approximately 1200 Hertz.

28. The inductance measurement circuit of Claim 1 wherein said demodulation circuit is a full-wave bridge rectifier.

29. The inductance measurement circuit of Claim 1 further comprising a heating element in close proximity to a capacitor of said pair of resistance-inductance-capacitance driver circuits.

30. The inductance measurement circuit of Claim 29 wherein said heating element is thermally coupled to said capacitor.

31. The inductance measurement circuit of Claim 29 wherein said heating element is a resistor connected to a variable current source.

32. The inductance measurement circuit of Claim 31 wherein said resistor and said capacitor are thermally insulated to improve thermal efficiency.

33. The inductance measurement circuit of Claim 1 wherein said analog-to-digital converter includes a low-pass filter.

34. The inductance measurement circuit of Claim 1 wherein said analog-to-digital converter includes differential inputs and rejects a common-mode noise originating from the wire-loop.

35. The inductance measurement circuit of Claim 1 wherein a characteristic of each said pair of resistance-inductance-capacitance driver circuits is modulated to balance said pair of resistance-inductance-capacitance driver circuits for common-mode noise rejection.